

## Guest Editorial

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Advances in process technology today are enabling a profound increase in the number of applications that can be realized using Programmable Logic Devices (PLDs), but along with this technology advances come new design challenges. Programmable devices are becoming increasingly attractive for a broader range of applications, from networking and telecommunications to high volume consumer products. The underlying ultra deep submicron technology that makes this possible, however, presents new and challenging problems for designers. The sheer sizes of designs that can be implemented produce lengthy software runtimes and exceed the memory available in computers. Additionally, the physical interconnections between logic elements now dominate IC delay, and high productivity design methods such as conventional logic synthesis fail to adequately account for these effects.

Today, PLDs are addressing a rapidly expanding number of applications. Shorter design cycles, lower development cost, and increasing parity of gate count, cost and performance are making PLDs attractive alternatives to ASIC implementation. In particular, networking and telecommunications applications are increasingly materializing in programmable devices. The fast turnaround and low entry cost of PLDs make them ideal choices for dynamic markets such as networking and telecommunications that are characterized by rapidly changing standards and increasingly narrow market windows. With the increasing gate counts, and new system-level features in contemporary PLDs, programmable devices may indeed surpass ASIC as the preferred implementation method for these market segments.

In this special issue, eight outstanding papers address various aspects of PLD design. The first paper deals with logic synthesis in “BDD-Based Logic Synthesis for LUT-Based FPGAs.” The next paper “Reduction Design for Generic Universal Switch Blocks” deals with an important topic of PLD architectural design: switchbox design. SAT-based solvers are becoming popular in handling complex CAD problem. Recent conferences such as ICCAD 2002 devoted special sessions to this topic. The next paper, “Run-Time Performance Optimization of an FPGA-Based Deduction Engine for SAT Solvers,” deals with the issue of an FPGA-based SAT solver.

The next two papers tackle PLD issues at higher levels: the first one “Behavioral Synthesis of Field Programmable Analog Array Circuits” deals with the behavioral level and the second one “Instruction Generation for Hybrid Reconfigurable Systems” deals with the compiler level.

ASIC Physical design tools are more advanced than their PLD counterparts, perhaps because physical design for PLDs started later than that for ASICs. Nevertheless, physical design for PLDs has some unique challenges. The next three papers deal with physical design aspects of PLDs. These papers are: “Performance-Driven Placement for Dynamically Reconfigurable FPGAs,” “Efficient Circuit Clustering for Area and Power Reduction in FPGAs,” and “A Search-Based Bump-and-Refit Approach to Incremental Routing for ECO Applications in FPGAs.”

Multi-million gate capacity and clock speeds approaching 200 MHz for PLD-based designs are coming into the mainstream, and the Electronic Design Automation technology that supports these applications is significantly behind. PLD devices are now being fabricated in advanced, ultra deep submicron technology, and along with the multi-million gate IC capacity enabled by this technology come new and difficult design problems: design size and complexity, and interconnect-dominant delay. As witnessed when high gate count deep submicron ASIC designs first emerged, size significantly impacts software runtime and the redominance of interconnect between logic elements have a major impact on PLD device performance. We hope this special issue motivates more researchers in academia, industry, (and startups!) to work in CAD tools for complex PLDs of present and the future.

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